What is claimed is:

1. An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a general purpose register used for the arithmetic operation of a CPU and having the function of receiving, delivering and storing the data;

a secure information unit added to the general purpose register and adapted to be set to the state not requiring security in the case where the data is transferred from the user memory space to the data unit of the general purpose register, and adapted to be set to the state requiring security in the case where the data is transferred from the secure memory space to the data unit of the general purpose register;

a data control unit having the function of determining whether the value of the secure information unit is in the state requiring security or the state not requiring security when the data of the general purpose register is written in the user memory space, thereby determining whether the data transfer to the user memory space is prohibited or not; and

an address control unit having the function of determining which of the user memory space and the secure memory space is indicated by the address information, and selecting the value of the secure information unit.

2. An information processing apparatus according to claim 1, comprising:

an instruction fetch address control unit having the function of determining which of the user memory space and the secure memory space is indicated by the address information when storing the instruction code input from

the data control unit, and the function of notifying the data control unit which of the user program and the secure program is under execution;

an instruction buffer used by the CPU to fetch an instruction and having the function of storing therein the instruction code input from the data control unit;

a user program arranged in the user memory space and adapted to be generated mainly by the user; and

a secure program arranged in the secure memory space and adapted to be generated mainly by the developer, the contents of the secure program being not disclosed to the user;

wherein the data control unit executes the data transfer from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction in such a manner that the data transfer to the user memory space is prohibited in the case where the instruction fetch address control unit determines that the instruction is fetched from the user memory space and the value of the secure information unit is in the state requiring security.

3. An information processing apparatus according to claim 2, comprising:

a plurality of general purpose registers used for the arithmetic operation of the CPU, and having the function of receiving and delivering the data from and to the data control unit, and storing the data therein;

a plurality of secure information units added to the general purpose registers, respectively, and under the control of the address control unit, adapted to be set to selected one of the state requiring security, the state not requiring security and the state of invalid security; and

a general purpose register file having such a function that in performing the arithmetic operations between at least two of the general purpose registers in compliance with an operating instruction, the secure information unit of one of the general purpose registers for storing the result of the arithmetic operation is set to the state of invalid security in the case where the value of the secure information unit of at least one of the general purpose registers is in the state requiring security;

wherein the data control unit issues an operating instruction to the general purpose register with the secure information unit in the state of invalid security in such a manner as to prohibit the arithmetic operation in the case where the instruction fetch address control unit determines that the operating instruction has been fetched from the user memory space.

4. An information processing apparatus according to claim 2, comprising a status register used for the arithmetic operation of the CPU and having the function of holding the value of the result of the comparative arithmetic operation as a comparative flag, the status register further having the function of keeping the value of each flag unchanged in the case where at least one of the general purpose registers has the value of the secure information unit in the state requiring security at the time of the arithmetic operation executed between at least two of the general purpose registers in compliance an operating instruction and the instruction fetch address control unit determines that the operating instruction has been fetched from the user memory space.

5. An information processing apparatus according to claim 2, comprising:

a read/write user IO space used for accessing the user memory space from outside;

a read/write secure IO space used for accessing the secure memory space from outside;

an IC card used connected to the secure IO space and having the function of storing the data including a debug key therein; and

a debug key stored in the IC card and having such a function that when read out by the CPU through the secure IO space when the developer debugs the secure program with the user system, the address determining function of the instruction fetch address control unit and the address control unit is stopped;

wherein the data control unit has such a function that the data transfer to the user memory space is not prohibited in the case where the debug key is read by the CPU when transferring the data from the data unit of the general purpose register to the memory spaces in compliance with a transfer instruction and at the same time in the case where the instruction is fetched from any one of the user memory space and the secure memory space.

6. An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering the data with secure information into a general purpose register with secure information having the function of receiving and holding the data with secure information;

a built-in RAM space for receiving and holding the data with secure information from the general purpose register and delivering the data thus held to the general purpose register; and

a data output control unit having the function of controlling the data transfer to an external space by the secure information;

wherein the data output control unit performs the control operation to determine whether the data transfer to the external space is prohibited or not by the value of the secure information set in the general purpose register.

7. An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with secure information into a general purpose register with secure information having the function of receiving and holding the data with secure information, and delivering an instruction with secure information into an instruction decoder with secure information having the function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

a built-in RAM space with secure information for receiving and holding the data with secure information from the general purpose register and delivering the data thus held to the general purpose register;

an interrupt saved information unit with secure information having the function of adding, upon generation of an interrupt process, the secure information of the

instruction decoder to the data saved in the stack area of the built-in RAM space; and

a data output control unit having the function of controlling the data transfer to an external space by the secure information;

wherein the data output control unit performs the control operation to determine whether the data transfer to the external space is prohibited or not by the value of the secure information set in the general purpose register.

8. An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with secure information into a general purpose register with secure information having the function of receiving and holding the data with secure information, and delivering an instruction with secure information into an instruction decoder with secure information having the function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

a built-in RAM space with secure information having the function of receiving and holding the data with secure information from the general purpose register and delivering the data thus held to the general purpose register;

an interrupt saved information unit with secure information having the function of adding, upon generation of an interrupt process, the secure information of the instruction decoder to the data saved in the stack area of

the built-in RAM space;

a stack pointer for defining a part of the built-in RAM space as a stack area; and

a saved information rewrite control unit for controlling the operation of rewriting the stack area of the built-in RAM space;

wherein the saved information rewrite control unit prohibits the rewrite operation in the case where the instruction of the instruction decoder is associated with the user memory space and intended to rewrite the stack area of the built-in RAM space.

9. An information processing apparatus for accessing memory spaces including a user memory space and a secure memory space, comprising:

a DMA with secure information having the function of holding the secure information;

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering the data with secure information into the DMA;

a built-in RAM space for receiving and holding the data with secure information from the DMA and delivering the data thus held to the DMA; and

a data output control unit having the function of controlling the data transfer to an external space by the secure information;

wherein the data output control unit performs the control operation to determine whether the data transfer to the external space is prohibited or not by the value of the secure information set in the general purpose register.

10. An information processing apparatus for accessing

memory spaces including a user memory space and a secure memory space, comprising:

a secure information generating unit for determining which of the user memory space and the secure memory space is indicated by address information, and delivering data with secure information into a general purpose register with secure information having the function of receiving and holding the data with secure information, and delivering an instruction with secure information into an instruction decoder with secure information having the function of determining which of the user memory space and the secure memory space is associated with the instruction under execution;

an operating unit with secure information having the function of reflecting the secure information of the instruction decoder in the arithmetic operation executed in accordance with the instruction decoded by the instruction decoder; and

a data output control unit having the function of controlling the data transfer to an external space by the secure information;

wherein the data output control unit performs the control operation to determined whether the data transfer to the external space is prohibited or not by the secure information set in the general purpose register and the secure information set in the operating unit.